REMARKS

The Examiner objected to the drawings because they did not include reference signs mentioned in the description. Attached hereto applicant is submitting a proposed drawing correction to FIGS. 1, 7 and 10. These proposed corrections are shown in red ink.

The objections raised by the Examiner in the specification have been corrected.

The Examiner objected to claims 88, 96 and 101 because of various informalities. These informalities have been corrected.

Claims 10-18 and 88-104 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which is not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. As pointed out in the Office action, applicants elected the invention of FIG. 1. In FIG. 1, block 30 is labeled as "Acquisition/Tracking Loops,". However, these loops are shown in detail in FIGS. 4, 5, 7 to 16, and 18 to 25. Thus, as illustrated below in the discussion of the correspondence between claim elements and drawing elements, the configuration of claims 10-18 and 88 to 104 do correspond to the elected embodiment of FIG. 1, because FIG. 1 incorporates the details of FIGS. 4, 5, 7 to 16, and 18 to 25. In summary, applicant is claiming only a single invention in all the claims presented for examination.

(a) With reference to FIG. 4, in claim 1 the first nested tracking loop corresponds to LF Inside 66, DDFS Inside 70, and mixer 58, the second nested tracking loop corresponds to LF Outside 68, DDFS Outside 72, and mixer 50, and the third tracking loop corresponds to baud LF 78, baud DDFS, and HB/VID 52.

(b) With reference to FIG. 5, in claim 12 the first high pass filter corresponds to Nyquist prefilter 62 and the second low pass filter corresponds to Nyquist prefilter 54.

(c) With reference to FIG. 7, in claim 18 the phase/frequency detector corresponds to baud PD 76, the means for determining whether the pilot is centered corresponds to baud LF 78 and summing node 80, and the oscillator circuit corresponds to baud NCO 82.

(d) With reference to FIGS. 5 and 9, in claims 88, 96, and 100 the equivalent filter corresponds to bandpass 74, the decision directed carrier phase recovery loop corresponds to equalizer 24, LF Outside 68, outside NCO 72, and mixer 50, and the phase detector corresponds to QAM PD 120 and VSB PD 122.

(e) With reference to FIG. 22, in claims 88, 96, and 100 the maximum likelihood sequence estimation circuit corresponds to slicer 310.

(f) With reference to FIG. 12, in claim 92 the real to imaginary signal converter corresponds to Hilbert transform 180 and the time compensation circuit corresponds to baud NCO 80 and HB/VID 52 and in claims 93 to 95 the Hilbert transform filter corresponds to Hilbert transform 180.

In view of the foregoing information, it is submitted that claims 10-18, 88 to 104 meet the requirements of 35 U.S.C. § 112, first paragraph. These claims also stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The foregoing correspondence between claim elements and the elements disclosed in the drawings also demonstrates that these claims meet the requirements of section 112, second paragraph.

In view of the amendments made at this time and the foregoing remarks, reconsideration of claims 10-18 and 88 to104, and allowance of this application are requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By _____

LeRoy T. Rahn
Reg. No. 20,356
626/795-9900

LTR/mas

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Page 1, third paragraph, lines 22-32, amend to read as follows:

BACKGROUND OF THE INVENTION

Modern digital telecommunication systems are operating at ever-increasing data rates to accommodate society's growing demands for information exchange. However, increasing the data rates, while at the same time accommodating the fixed bandwidths allocated by the Federal Communications Commission (FCC), requires increasingly sophisticated signal processing techniques. Since low cost, small size and low power consumption are ~~portent~~ important in the hardware implementations of such communication systems, custom integrated circuit solutions are important to achieving these goals.

Page 9, eighth paragraph, lines 16-34 through page 10, lines 3-4, amend to read as follows:

DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed to digital data communication systems and methods for operating such systems in order to synchronize a receiver's timebase to a remote transmitter's. Carrier frequency and symbol timing information ~~is~~ are recovered from a pilot (unsuppressed carrier) signal that is inserted into a VSB spectrum, in contrast to conventional timing recovery systems, which recover timing information from the segment sync signal that is provided at the end of every line of 828 symbols, and is specifically designed to facilitate timing recovery.

Page 20, third paragraph, lines 17-28, amend to read as follows:

In-phase (I) and quadrature phase (Q) baseband signals are then filtered by square-root Nyquist filters 22 which can accommodate roll-off factors of 11-18%. The outputs of the square-root Nyquist filters are subsequently directed to an adaptive equalization block 24 and are parallel-processed by a Nyquist-type prefilter 26 to provide an input signal to an acquisition/tracking loop circuit ~~28~~ 30 which includes carrier recovery loop circuitry to support carrier frequency recovery and spectrum centering as well as baud recovery loop circuitry, for symbol timing extraction, as will be described in greater detail below.

Page 21, second paragraph, lines 13-22, amend to read as follows:

While the square-root Nyquist filters ~~28~~ 22 ordinarily assure that there is a minimal inter-symbol interference (ISI) over a perfect channel, the Nyquist filters are unable to remove ISI due to the imperfect channel characteristics. Accordingly, the dual mode QAM/VSB receiver according to the invention, provides an adaptive, multi-tap decision directed equalizer circuit 24, having 64 feedforward taps and 432 feedback taps, which is sufficient to remove ISI components generated by worst-case coaxial cable and terrestrial broadcast channels with multi-path spreads of up to 40 μsec at 10.76 Mbaud.

Page 22, first paragraph, lines 3-17, amend to read as follows:

The dual mode QAM/VSB receiver exemplified in FIG. 1 further includes a forward error correction (FEC) and decoder block 32, which is compatible with all common CATV standards and the ATSC terrestrial broadcast standard. Specifically, the Annex A/C decoder circuitry implements four general functions, frame synchronization, convolutional deinterleaving, ~~reed-Solomon~~ Reed-Solomon error correction and derandomization. Hard decisions are input to the frame synchronizer which locks onto the inverted synch byte pattern, conventionally provided in television data frames. After synchronization, data interleaving is removed by a convolutional deinterleaver utilizing a Ramsey type III approach. Data symbols are next provided to a Reed-Solomon decoder, which is able to correct up to 8 symbol errors per RS block, followed by data derandomization to undo the corresponding randomization operation of the transmitter's modulator.

Page 25, last paragraph, lines 32-35 through page 26, lines 3-10, amend to read as follows:

The dual mode QAM/VSB receiver in accordance with the invention is capable of operating on transmitted signals modulated by any of the above modulation formats with substantially the same circuitry. Particularly, and where ~~appripriate~~ appropriate, the receiver treats VSB modulated signals as though they were OQAM because of the frequency shift relationship therebetween. Where signals are required to be treated as VSB signals, processing blocks include a real to imaginary converter circuit, in particular a Hilbert transform filter, which creates an analogue Q rail signal from the VSB real I rail, in order to use complex circuitry which directly extracts an error vector quantity.

Page 29, first paragraph, lines 3-17, amend to read as follows:

It will thus be understood that there are two stages to carrier acquisition, a first stage, termed "an outside stage" (or outside loop) provides for mixing the received digitized spectrum down to baseband and which might properly be termed "a tracking loop", and a second correction stage, termed "an inside loop", which functions more as an acquisition loop and which provides a correction factor to the spectrum to make sure the spectrum is properly centered. In addition, the correction factor is "leaked" from the inside loop to the outside loop in order that the inside loop might be constructed with a wide bandwidth, typically in the 100 kHz range in order to provide for fast acquisition. Correction factors are leaked to the outside loop such that the outside loop might be constructed with a relatively narrow bandwidth in order to provide for more accurate tracking ~~capability. Once~~ capability once the carrier has been acquired.

In the Claims:

~~CLAIMS~~

WHAT IS CLAIMED

12. The digital communication system according to claim 11, wherein symbol timing is performed at a sampling frequency, the system further comprising:

a first ~~high pass~~ filter having a high-pass characteristic and a lower cut-off frequency related to the sampling frequency;

a second ~~low pass~~ filter having a low pass characteristic and an upper cut-off frequency related to the sampling frequency; and

wherein the first and second filters define an equivalent bandpass filter having symmetric passband regions centered about a frequency related to the sampling frequency.

88. (Amended) A digital communication system for receiving signals modulated ~~an~~ in accordance with a multiplicity of modulation formats, comprising:

a front end receiving an input spectrum at an intermediate frequency;

first and second nested carrier tracking loops, the first loop acquiring carrier frequency lock in operative response to a predetermined frequency component inserted into the received spectrum, the second loop providing a signal adapted to position the spectrum at a predetermined location relative to baseband in operative response to said predetermined frequency component;

a third tracking loop coupled to define a symbol timing parameter in operative response to said same predetermined frequency component;

an equivalent filter operating on the received spectrum in order to define a pair of symmetric signals, each of the symmetric signals centered at the characteristic frequency of the predetermined frequency component when the received spectrum is at baseband;

a decision directed carrier phase recovery loop having a phase detector operative with respect to each of the multiplicity of modulation formats;

~~a single bit LMS derotator coupled to adjust phase offset of signals directed to an adaptive decision feedback equalizer;~~

an adaptive decision feedback equalizer, including;

a feedforward filter;

a decision feedback filter; ~~and~~

a single bit LMS derotator coupled to adjust phase offset of signals directed to the adaptive decision feedback equalizer; and

a maximum likelihood sequence estimation circuit, coupled to receive input symbol samples from the feedforward filter, the maximum likelihood sequence estimation circuit integrated into a timing loop so as to provide enhanced reliability symbolic decisions to an input of the timing loop.

96. (Amended) A digital communication system for receiving signals modulated ~~an~~ in accordance with a multiplicity of modulation formats, comprising:

a front end receiving an input spectrum at an intermediate frequency;

first and second nested carrier tracking loops, the first loop acquiring carrier frequency lock in operative response to a pilot frequency component inserted into the received spectrum, the second loop providing a signal adapted to position the spectrum at a predetermined location relative to baseband in operative response to said pilot frequency component;

a third tracking loop coupled to define a symbol timing parameter in operative response to said same pilot frequency component;

an equivalent filter operating on the received spectrum in order to define a pair of symmetric signals, each of the symmetric signals centered at the characteristic frequency of the pilot frequency component when the received spectrum is at baseband; and

a decision directed carrier phase recovery loop having a phase detector operative with respect to each of the multiplicity of modulation formats.

101. (Amended) A digital communication system for receiving signals modulated ~~an~~ in accordance with a multiplicity of modulation formats, comprising:

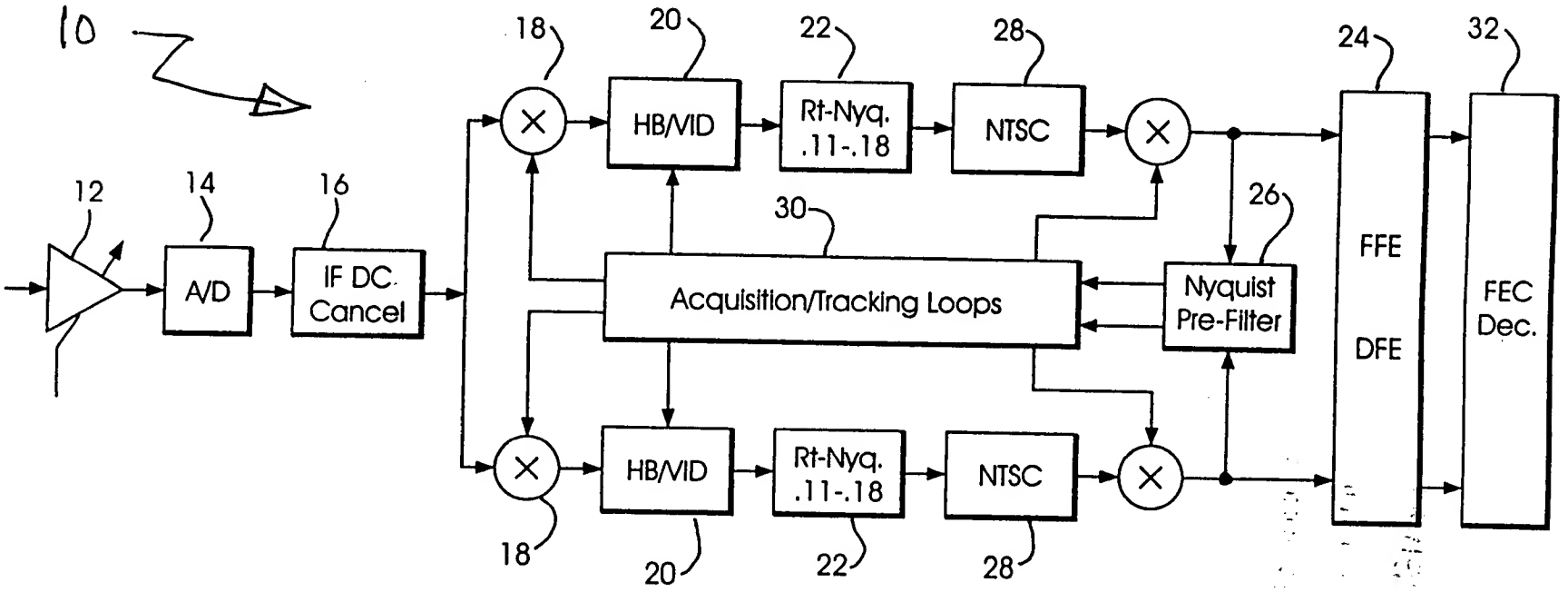
reference synthesizer circuits;

a front end receiving an input spectrum at an intermediate frequency;

first and second nested carrier tracking loops;

a symbol timing loop; and

wherein the tracking and timing loops control the reference synthesizer circuits in operative response to a passband signal centered at a frequency characteristic of an inserted pilot signal.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12
14
16
A/D
IF DC
Cancel
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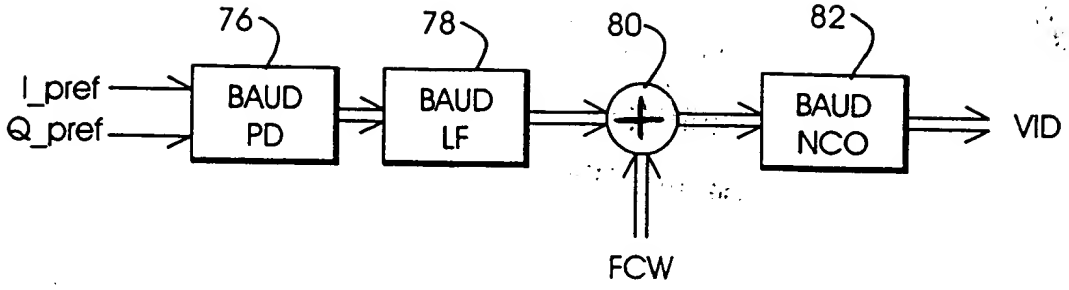
20
22
28
HB/VID
Rt-Nyq.
.11-.18
NTSC
30
Acquisition/Tracking Loops
26
Nyquist
Pre-Filter
24
32
FFE
DFE
FEC
Dec.
18
20
22
28
HB/VID
Rt-Nyq.
.11-.18
NTSC

FIG. 1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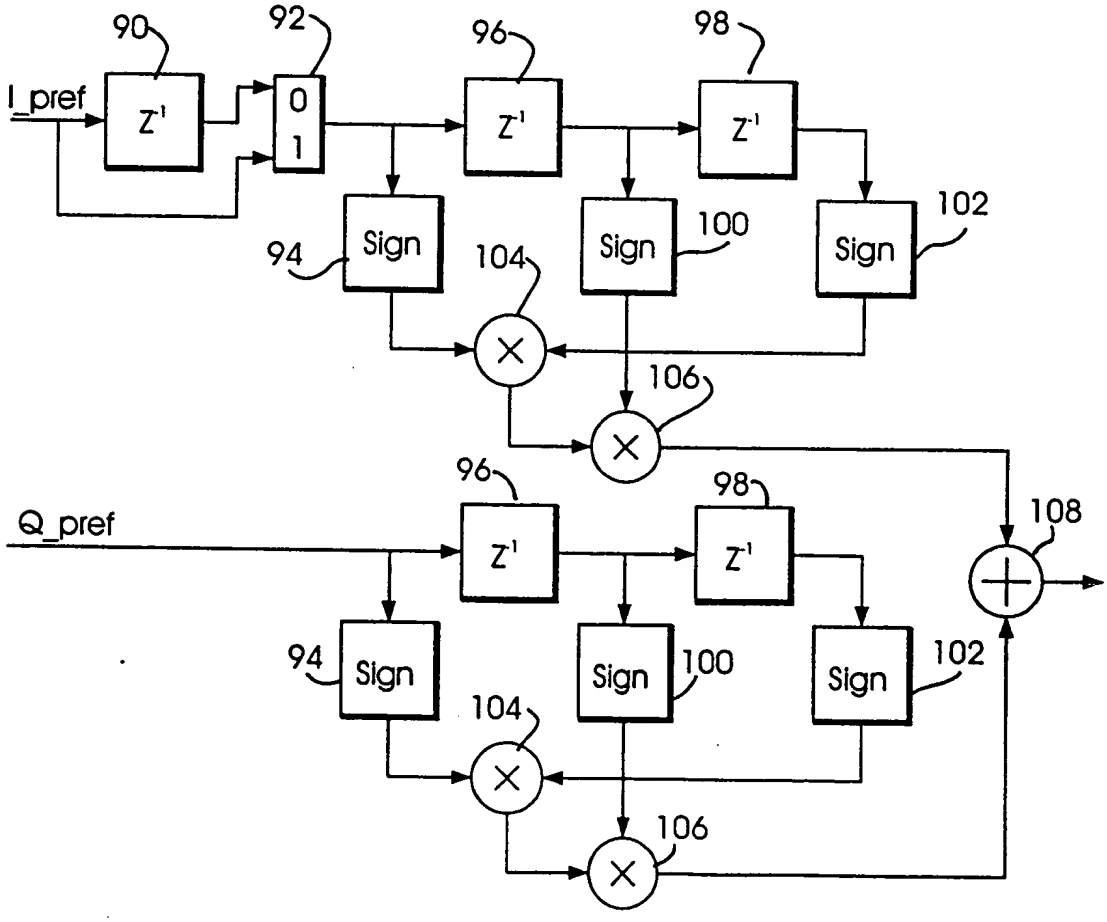
80
82
I_pref
Q_pref
BAUD PD
BAUD LF
BAUD NCO
VID
FCW

FIG. 7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92
96
98
I_pref
Z-1
0
1
Sign
94
100
102
104
106
Q_pref
108

FIG. 8

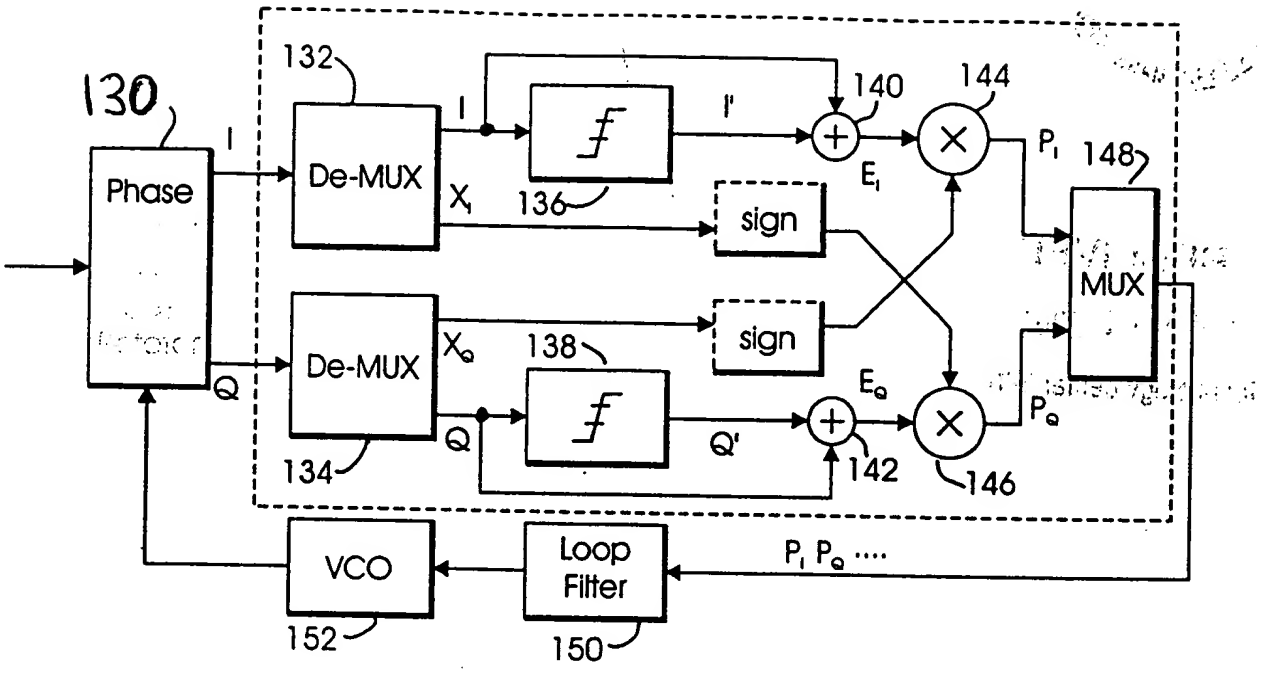
130
132
Phase
I
Q
De-MUX
De-MUX
X_I
X_Q
134
136
138
I'
Q'
sign
sign
140
142
144
146
148
E_I
E_Q
P_I
P_Q
MUX
VCO
Loop Filter
P_I P_Q ....
152
150

FIG. 10

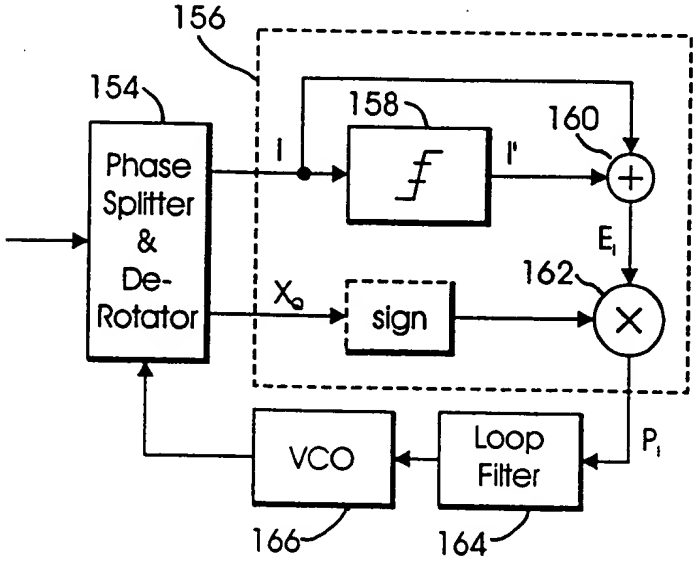
156
154
Phase Splitter & De-Rotator
158
160
I
I'
E_I
162
X_Q
sign
VCO
Loop Filter
P_I
166
164

FIG. 11